HONOURS

U.G. 4th Semester Examination - 2021

BCA

Course Code : BBCASEHT405

Course Title: Computer Organization

Full Marks : 50 Time : 2 Hours

The figures in the right-hand margin indicate marks.

Answer all the questions by choosing correct alternative: 2×25=50

1. In computer, subtraction is done by –
   a) 10's complement
   b) 9's complement
   c) 1's complement
   d) 2's complement
2. The decoded instruction is stored in _____
   a) IR
   b) PC
   c) Registers
   d) MDR
3. A stack organized computer system use instruction of –
   a) Indirect addressing
   b) Two adressing
   c) Zero addressing
   d) Index addressing

4. During the execution of a program which gets initialized first?
   a) MDR
   b) IR
   c) PC
   d) MAR
5. A group of bits that tell the computer to perform a specific operation is known as –
   a) Instruction code
   b) Microoperation
   c) Accumulator
   d) Register
6. The registers, ALU and the interconnection between them are collectively called as _____
   a) process route
   b) information trail
   c) information path
   d) data path
7. Which one of the following is the address generated by the CPU?
   a) Physical address
   b) absolute address
   c) logical address
   d) None of these

8. A source program is usually in _____

   a) Assembly language

   b) Machine level language

   c) High-level language

   d) Natural language

9. The circuit used to store one bit data is known as –

   a) Register

   b) Encoder

   c) Decoder

   d) Flip Flop

10. The ALU makes use of _____ to store the intermediate results.

   a) Accumulators

   b) Registers

   c) Heap

   d) Stack

11. Cache memory acts between –

   a) CPU & RAM

   b) RAM & ROM

   c) CPU & Hard disk

   d) None of these

12. The Input devices can send information to the processor.

   a) When the SIN status flag is set

   b) When the data arrives regardless of the SIN flag

   c) Neither of the cases

   d) Either of the cases

13. An n-bit microprocessor has –

   a) n-bit program counter

   b) n-bit address register

   c) n-bit ALU

   d) n-bit instruction registor

14. To reduce the memory access time we generally make use of _____

   a) Heaps

   b) Higher capacity RAM's

   c) SDRAM's

   d) Cache's

15. An instruction pipeline can be implemented by means of –

   a) LIFO buffer

   b) FIFO buffer

   c) Stack

   d) None of the above

16. In the case of, Zero-address instruction method the operands are stored in _____

a) Registers

b) Accumulators

c) Push down stack

d) Cache

17. Memory unit accessed by content is called –

a) Read only memory

b) Programmable memory

c) Virtual memory

d) Associative memory

18. The addressing mode/s, which uses the PC instead of a general purpose register is _____

a) Indexed with offset

b) Relative

c) Direct

d) Both Indexed with offset and direct

19. What is the content of stack pointer?

a) address of the current instruction

b) address of the next instruction

c) address of the top element of the stack

d) Size of the stack

20. When generating physical addresses from a logical address the offset is stored in _____

a) Translation look-aside buffer

b) Relocation register

c) Page table

d) Shift register

21. In which addressing mode the operand is given explicitly in the instruction?

a) Absolute

b) Immediate

c) Indirect

d) Direct

22. Complete the following analogy:- Registers are to RAM's as Cache's are to _____

a) System stacks

b) Overlays

c) Page Table

d) TLB

23. Data hazards occur when –

a) Greater performance loss

b) Pipeline changes the order of read write access to operand.

c) Some functional unit is not fully pipelined

d) Machine size is limited

24. A 24 bit address generates an address space of _____ locations.

a) 1024

b) 4096

c) 248

d) 16,777,216

25. When more than one processes are running concurrently on a system.

a) batched system

b) real time system

c) multiprogramming system

d) Multiprocessor system

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